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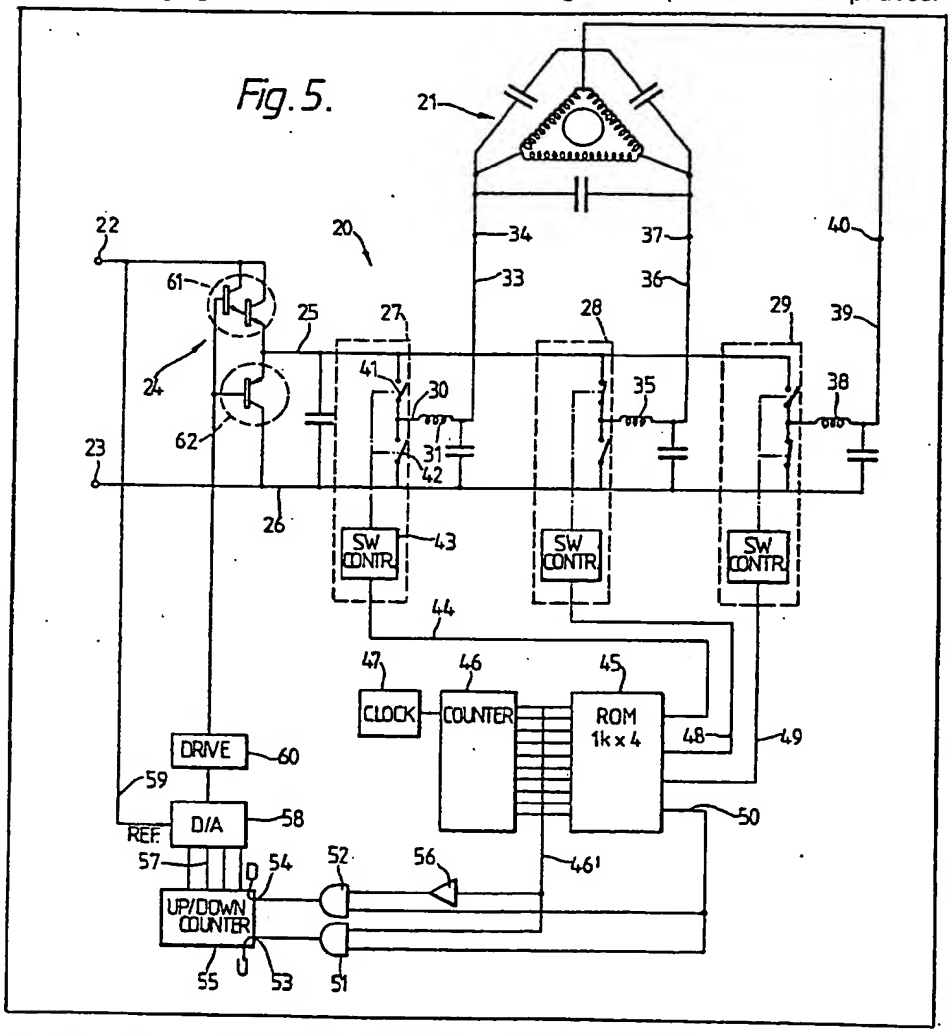
(54) A three phase supply synthesis arrangement

(57) The arrangement comprises switching means 27—29 across a d.c. supply bus 25, 26 for each phase, the switching means having series connected switches 41, 42 conditionable to be closed alternately throughout the synthesised cycle so that a junction point 30, connected to the load, is maintained at the higher bus potential for one-third of the cycle, maintained at the lower (ground) bus potential for a non-contiguous one-third of the cycle, and varied from the higher to lower bus potential, and vice versa, in intervening one-sixths of the cycle by rapidly changing the switch states to vary the average junction potential. The conditioning of each switching means is controlled by a ROM 45 containing the switch conditions for points throughout the cycle and accessed sequentially by a counter 46 to synthesise a signal having a trapezoidal waveform approximating to a sinusoidal signal (Figure 3) but because the switching means spends a large part of each cycle without changing state there are a few power losses. To approximate more closely to a sinusoidal signal (Figure 4) without increasing switching activity the ROM 45 also stores data read synchronously with the switching data to be converted to an analogue crest function which modulates the level of the higher bus potential for all phases.

Fig. 5.



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The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

Fig.1.

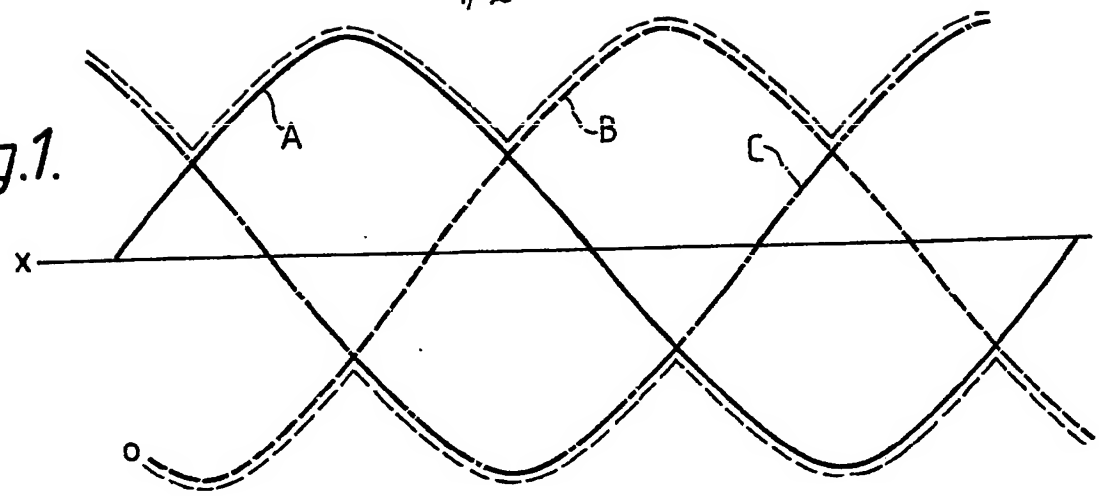


Fig.2.

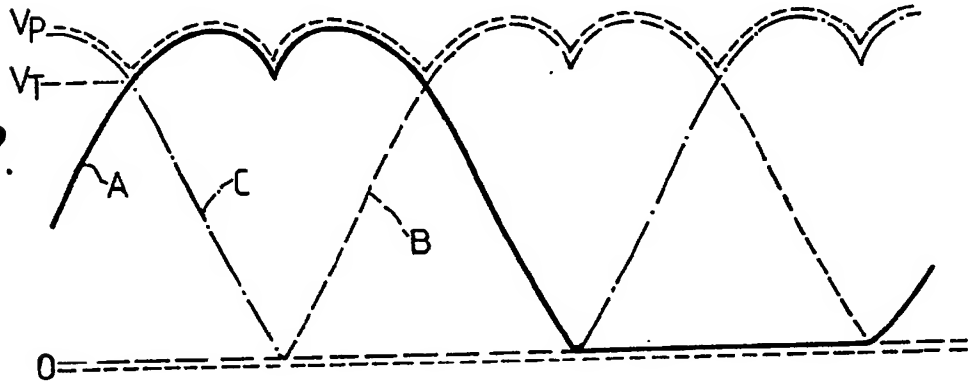


Fig.3.

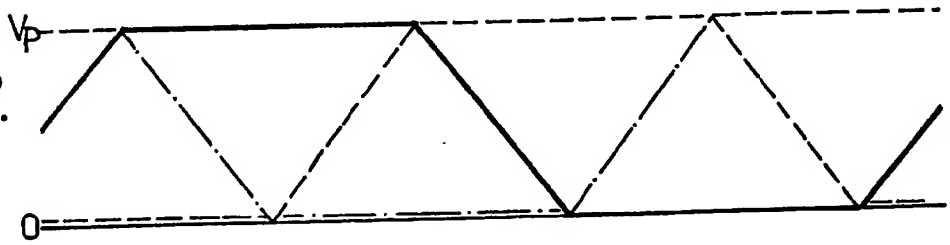


Fig.4.

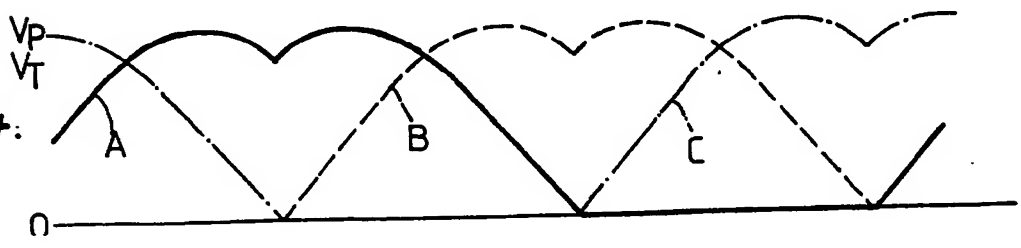
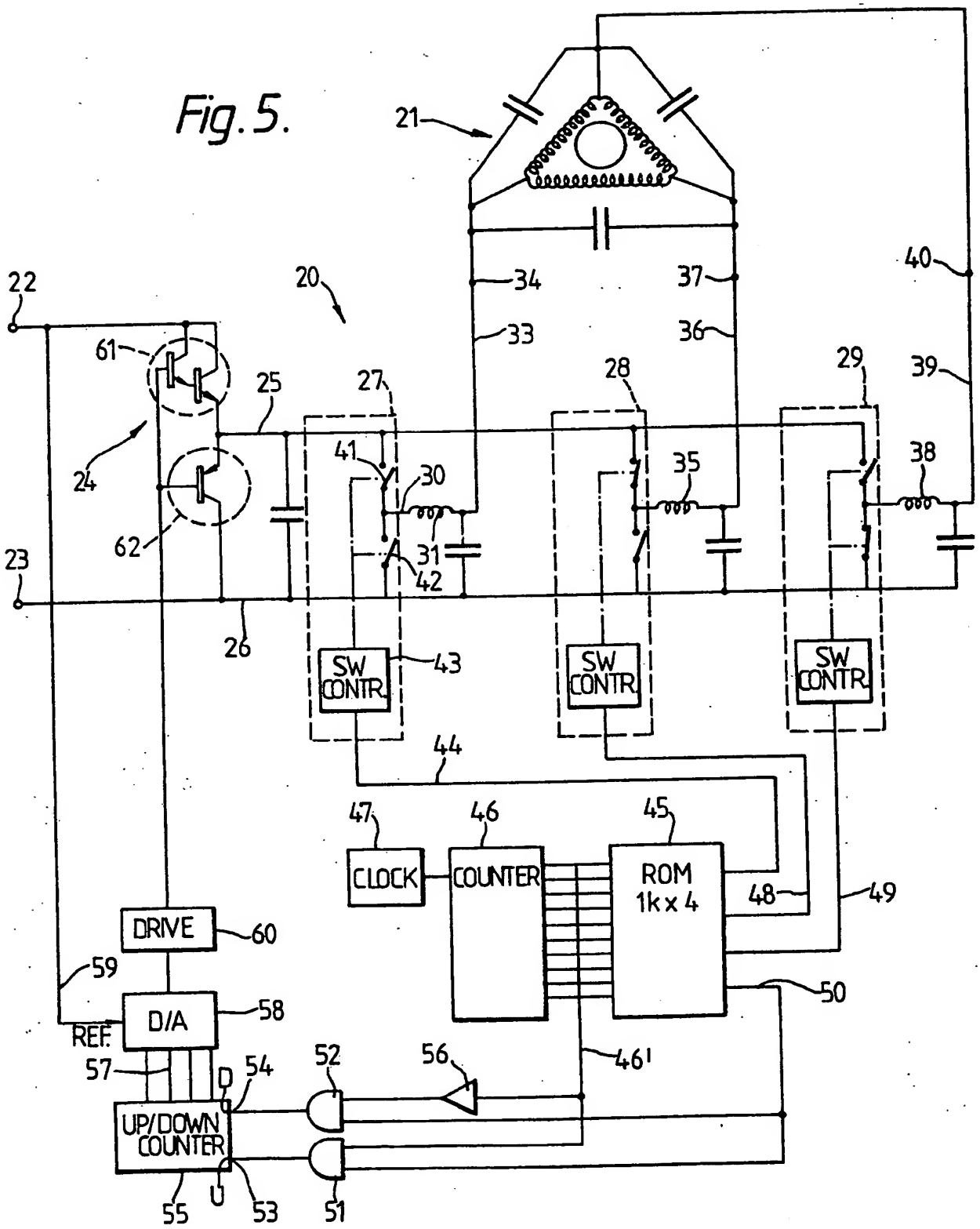


Fig. 5.



SPECIFICATION

Multiple phase supply systems

This invention relates to multiple-phase supply systems for electric motors and like loads and in particular to systems in which a multiple-phase supply is synthesised from a d.c. supply.

It is known to synthesise multiple (usually three) phase supply voltages for motors and like loads by associating with each load supply terminal a filter connected to the junction between a pair of switches connected in series across a d.c. supply. By opening and closing the switches of each pair alternately an average value of voltage which is a fraction of the d.c. supply voltage is applied to the associated terminal and varied in accordance with a predetermined function to effect a three phase supply. Known arrangements of this form have a number of characteristics which may be disadvantageous where supply voltage is limited or power limitations demand minimal dissipation in the form of heat or where packing density requires such losses to be minimised.

One of the major problems with switches thus connected, which in practice are usually semiconductor devices, has been the generation of heat during switching. One principal source of heat generation is caused by brief simultaneous conduction by both switches. A drive arrangement which substantially eliminates such simultaneous conduction is described in co-pending application No. 81.31805 and which helps in achieving desirable characteristics.

However any switching action generates heat as a function of switching speed, voltage across the switch and the proportion of synthesised cycle spent in switching, that is, the number of switching operations. This latter factor is capable of exercising greatest effect and minimisation of switching operations has led to the generation of 'square-wave' approximations to a sinusoid. Such a square-wave approximation is high in harmonics which may affect the load e.g. in a motor produce eddy currents leading to the generation of undesirable heat which is to be avoided.

Also, although it is still generally required to provide a d.c. voltage level at least as great as the peak terminal-to-terminal voltage applied to the load, for most of the time a d.c. voltage level less than the peak is required, and excess heat generated during switching requires correspondingly higher component ratings. Alternatively a tuned circuit may be employed which in turn leads to problems with changes in frequency or load characteristics.

It is an object of the present invention to provide a three phase supply synthesis arrangement which mitigates some or all of the disadvantages of known arrangements.

It is a further object of the present invention to provide a three phase supply synthesis arrangement which by use of a relatively small number of inexpensive and readily available components is less complex and less costly than known arrangements.

According to the present invention a three phase supply synthesis arrangement includes a d.c. power supply bus associated with each load supply terminal, switching means associated with each supply terminal of the load arranged to switch the terminal either to an upper potential level of the d.c. supply bus or a lower potential level of d.c. supply ground, and control means able to operate upon each of said switching means in a repetitive cycle, equally displaced in phase from the others, to condition the switching means to a first state for a one-third portion of a synthesised wavelength to maintain the associated load supply terminal at the upper potential level, condition the switching means to a second state for a different non-contiguous one-third portion of a synthesised wavelength to maintain the associated load supply terminal at the lower potential level and in the intervals between said portions to condition the switching means to change states alternately to apply a potential to the associated load terminal which has an average value that varies between said upper and lower levels of adjacent portions in accordance with a predetermined ramp function.

Such an arrangement enables a three-phase trapezoidal signal, approximately to a sinusoidal signal, to be generated with minimal switching and minimal heat generation within the switching means, while having a lower harmonic content than conventional 'square' switched signal.

Such a trapezoidal signal may be further approximated to a sinusoidal signal, without increasing switching, by crest generating means operable to vary the level of the d.c. supply bus potential cyclically in accordance with a crest function of wavelength equal to one sixth of the synthesised wavelength to produce six crests in synchronism with said portions of the synthesised signal, the peak value of the bus potential being associated with the peaks of said crest function and a lower intermediate level of the bus potential being associated with troughs of said crest function.

An embodiment of the present invention applied to synthesis of a three-phase supply will now be described by way of example with reference to the accompanying drawings, in which:—

Figure 1 shows the waveform of a three phase signal composed of three sinusoidal waves equally displaced in phase, and the envelope of the combined signal.

Figure 2 shows the signal of Figure 1 modified by clamping the level of one edge of the envelope.

Figure 3 shows the waveform of a three-phase signal approximating crudely to that of Figure 2, synthesised by switching a single d.c. supply in accordance with the present invention,

Figure 4 shows the waveform of the synthesised signal of Figure 3 modified to provide a closer approximation to the three-phase signal of Figure 2 by addition of a crest function, and

Figure 5 is a block diagram of a three phase supply synthesis arrangement according to the

present invention shown with a delta-connected motor as a load.

Referring to Figure 1 the combined waveforms of three sinusoidal signals are shown superimposed and equally displaced in phase with respect to each other conveniently identified as phase A, phase B and phase C. One wavelength only of each signal is shown and said signals are of the type applied to supply terminals of a three phase load (such as a delta-connected gyro spin motor shown in Figure 5). The potential difference between load supply terminal inputs may be readily determined by examining the potential difference between the two corresponding phase waveforms.

The upper and lower edges of the composite waveform define an envelope emphasised by broken lines showing variations of the maximum amplitude of voltage required throughout the cycle.

The composite waveform is symmetrically positive and negative with respect to an arbitrary axis x and it will be appreciated that the composite waveform may be represented equivalently as a variation with respect to the lower edge O as shown in Figure 2. It will be seen from the envelope that the maximum phase-to-phase amplitude varies as a crest function waveform. For one cycle of the original signal the crest function waveform comprises a succession of six crests each representing a 60° segment disposed about the peak of the original sinusoidal wave and it can be shown by simple calculation that the envelope amplitude in the troughs (V_T) between crests is 87% of the peak amplitude (V_P).

Referring now to Figure 3, this shows three phases A, B and C of a synthesised supply crudely approximating to that of Figure 2. Each phase waveform is trapezoidal, one third of a portion of the wavelength being at an upper potential limit V_P with respect to a ground level limit O, a non-contiguous one-third portion of the wavelength being at the lower ground potential limit O and said portions being separated by two one-sixth portions where the waveform ramps between the upper and lower potential limits.

Each phase signal may be generated from a d.c. source of voltage V_P switched on continuously for the first one-third portion, off continuously for the second one-third portion and for the two one-sixth portions switched alternately between V_P and O to give an average voltage which is varied to provide the ramp functions.

Whereas such a waveform synthesis only crudely resembles a sinusoidal signal it has the advantage that for at least two-thirds of the signal cycle of each phase the voltage relative to lower limit O is at a steady level and power losses and heat generation due to switching are kept to a minimum.

In accordance with the present invention the synthesised waveforms may be approximated more closely to those originated sinusoidally in Figure 4 by modifying the level of the upper potential limit of the d.c. supply with a crest function as shown by the waveform of Figure 4. The waveform of the crest signal may be determined by calculation or measurement of values associated with a sinusoidally generated crest of Figure 2 or may be a coarser approximation thereof. Such a modification to the synthesised signals may be achieved independently of the switching associated with the synthesis of the basic trapezoidal functions and by reducing the upper potential limit to V_T in accordance with the maximum phase-to-phase amplitude requirements, minimises the unnecessary dissipation of power caused by applying phase voltages in excess of the minimum required to the switching means.

The ramp portions which are generated by switching may be linear and combine with the variation in d.c. supply level to produce bowed ramps (not shown) or may be given compensating non-linear characteristics in order to effect the linear ramps shown.

A circuit according to the present invention for providing three signals of such waveform as to form the composite signal of Figure 4 is shown in Figure 5 at 20 together with a load comprising a delta-connected gyro spin motor 21.

A d.c. supply of voltage V_P (not shown) is connected to a positive supply terminal 22 and ground terminal 23. The positive supply terminal 22 is connected by way of a potential dividing arrangement 24 to supply bus 25 and the ground terminal 23 is connected to a ground bus 26.

Connected between buses 25 and 26 are three separate switching means 27, 28 29. The switching means 27 has a switching output which is coupled by way of an inductor-capacitor filter network 31 to an output line 33 connected to a supply terminal 34 of the load motor 21. Switching means 28 feeds by way of a similar filter network 35 and an output line 36 connected to a load supply terminal 37 and switching means 29 feeds by way of filter network 38 to output line 39 connected to load supply terminal 40.

The switching means 27 comprises a pair of switches 41, 42 connected in series with each other between supply buses 25 and 26, the junction between the switches being connected to switching output 30. The switches open and close under control of a switch controller 43 which operates the switches such that when switch 41 is closed switch 42 is opened, and vice versa. The condition of the switch states is determined by the presence or absence of a control signal on a control line 44, that is, a binary '1' or '0' state.

The switching means 27 may take or be based on any suitable form involving mechanical or semiconductor switches, such as that described in the aforementioned co-pending application No. 81. 31805.

The switching means 28 and 29 are identical to switching means 27. The switching means 27—29 are conditioned by control signals stored on a memory which conveniently comprises a 1K ROM 45. The ROM has 1024 four-bit addresses which may conveniently be arranged for each

address to store one-bit data for four separate channels.

The ROM addresses are accessed by parallel-outputs of a 10-bit counter 46 which counts clock pulses generated by a clock 47. The counter 46 may be considered as a memory address counter. The clock pulse repetition rate is such that 2^{10} (= 1024) pulses are generated for each cycle of the synthesised signal and for each pulse the counter level increases by one, accessing a fresh address of the ROM to give outputs on four channels, one of which represents the control input 44 of switching means 27. Two other output channels represent corresponding control input lines 48, 49 of switching means 28 and 29 respectively and the fourth output channel 50 is associated with the crest function and will be referred to later.

On each of the three switching means control channels 44, 48 and 49 the single bit of data, a '0' or '1' conditions the associated switch states as appropriate at different count levels to represent the displacement between phases. For each channel, for two-thirds of the count there will be only two continuing values while for the remaining one-third the values change between '0' and '1' as required to condition the switching means, the filtered voltage output therefrom applied to the load varying with the increasing clock pulse count with the desired profile of the ramp function.

It will be appreciated that the proportion of time in each cycle for which the switching means is undergoing a change of condition is relatively small and losses which occur principally as a result of switching are reduced to a minimum. Furthermore the major components of the hardware required to effect the generation of this crude approximation waveform comprises only the switching means 27—29, ROM 45, counter 46 and clock 47.

The present invention completes the synthesis of an effective sinusoidal supply by generating a crest waveform signal which modulates the potential difference between supply buses 25 and 26.

The crest waveform of Figure 4 discussed above is generated from data stored in the fourth channel of ROM 45. The addresses of ROM 45, accessed in turn by counter 46 for each count level making up the count of one cycle, each contain a single bit representation of no-change or an increment (or decrement) in the crest function relative to the preceding count level so that throughout the cycle the ROM generates data representing a succession of six identical crests, the second (descending) part of each crest being a 'mirror image' of the first (ascending) part.

The fourth channel of the ROM is output on line 50 which connects by way of two AND gates 51, 52 to count-up and count-down inputs 53, 54 respectively of a subsidiary counter 55.

The AND gates 51, 52 also receive an input signal from the counter 46 fed directly to gate 51 and by way of an inverter 56 to gate 52. The effect of the gating arrangement is to apply ROM outputs to the count-up input 53 for the ascending parts of the crest function and to the count-down input 54 for descending parts.

The subsidiary counter 55 has a plurality of parallel outputs 57 which apply the instantaneous value of the subsidiary count to a D/A converter 58 which also receives a voltage reference input (V_p) 59 from supply terminal 22.

The output of the D/A converter 58 is an analogue signal which falls and rises in accordance with the desired crest function throughout the cycle. This analogue representation is applied to a drive circuit 60 which applies a drive signal to the potential divider circuit 24.

The potential divider circuit 24 essentially comprises a series connection of transistors of opposite conductivity types, 61, 62 to which the output of drive circuit 60 is applied such that the potential of bus 25 falls and rises with variation of the crest function from an upper or maximum supply limit V_p at a crest peak to an intermediate limit 87% of the upper limit, at a crest trough.

It will be seen that the variation of d.c. supply level with the crest function requires relatively few additional components for all phases.

There are twelve changes in crest direction for each cycle of the synthesised signal but the counter limit of 1024 does not form a convenient multiple from which to cause gating between count-up and count-down inputs of the subsidiary counter. The counter and ROM may be operated such that the full count is made a multiple of twelve, say 1020, from which gating signals can be derived at suitable count intervals. Alternatively some or all of the components of the crest function may be uneven in duration in terms of count numbers such that the total pulse count for one synthesis cycle of six crests is 1024. The precise means by which either of these two procedures may be implemented is open to choice and is illustrated only by the connecting line 46'.

It will be appreciated that the ROM space, while relatively inexpensive to purchase and implement is not necessarily used at its most efficient both on generating the trapezoidal waveforms and the crest waveform. In generating the trapezoidal waveforms there are relatively long periods within each cycle when successively accessed addresses contain unchanging data. If desired, the ROM may be used to define only the beginnings and ends of such periods, feeding signals to separate gating means (not shown) to supply control signals to the associated switching means under control of clock 47. Also, the crest function waveform is repetitive; if desired the data necessary to generate a single crest or half-crest only may be stored in the ROM with data causing repeated accessing as a function of the count.

Such variations may enable a smaller capacity ROM to be employed or a larger capacity counter to be driven at a higher clock rate.

A single four-channel ROM is of great practical convenience in simplifying synchronisation between channels where single-bit data

adequately defines the waveforms of each channel, but if multiple-bit data storage is necessary a larger capacity ROM or separate (synchronised) ROM's may be used.

It will be seen that irrespective of the precise nature of storing and accessing the relevant data the supply paths from the supply terminals 22 to the load are essentially d.c. coupled and thus independent of any frequency dependent components. The frequency of the synthesised three-phase signal may be varied between wide ranges merely by varying the frequency of clock 47. Also the amplitude of the synthesised signals is dependent only on the peak voltage V_p of the d.c. source applied to terminals 22 and 23. The crest waveform, generated as a percentage reduction is automatically scaled during the D/A conversion.

The above description relates to the load for the supply arrangement being provided by motor 21. It will be appreciated that the arrangement of the present invention is not restricted to a gyro spin motor but is suited to any load, bearing in mind that the simple filter networks 31, 35, 38 may need to be more elaborate if the load is not of an integrating nature.

It will further be appreciated that the present invention is not limited to synthesis of a three-phase supply, but with an appropriate number of switching means and corresponding number of memory channels containing phase displaced data and appropriate crest waveform data, supplies having different numbers of phases may be synthesised.

CLAIMS

1. A three-phase supply synthesis arrangement including a d.c. power supply bus associated with each load supply terminal, switching means associated with each supply terminal of the load arranged to switch the terminal either to an upper potential level of the d.c. supply bus or a lower potential level of d.c. supply ground, and control means operable upon each of said switching means in a repetitive cycle, equally displaced in phase from the others, to condition the switching means to a first state for a one-third portion of a synthesised wavelength to maintain the associated load supply terminal at the upper potential level, condition the switching means to a second state for a different non-contiguous one-third portion of a synthesised wavelength to maintain the associated load supply terminal at the lower potential level and in the intervals between said portions to condition the switching means to change states alternately to apply a potential to the associated load terminal which has an average value that varies between said upper and lower levels of adjacent portions in accordance with a predetermined ramp function.

2. A supply synthesis arrangement as claimed in claim 1 in which a single d.c. supply is arranged to supply potential to each of the load terminals.

3. A supply synthesis arrangement as claimed in claim 1 or claim 2 in which the predetermined relationship with which the average value of supply terminal potential varies is arranged to be substantially linear with time.

4. A supply synthesis arrangement as claimed in any one of claims 1 to 3 in which the control means includes a clock, a counter of clock pulses, memory means responsive to each of the counter levels to access a different address within the memory, data at each address representing the d.c. voltages to be applied to each load terminal at a particular point of the synthesised waveform corresponding to the count level associated with the address and drive means to read data from the memory for each address to condition the switching means to apply to each load terminal associated therewith the d.c. potential defined by the memory data for the duration of the address.

5. A supply synthesis arrangement as claimed in any one of the preceding claims in which the switching means comprises a pair of switches connected in series between the d.c. supply voltage and ground with their junction coupled to a switching output connected to the associated supply load terminal and drive means operable to close said switches alternately to connect the load either to the d.c. supply or supply ground.

6. A supply synthesis arrangement as claimed in any one of the preceding claims including crest generating means to vary the level of the d.c. supply bus potential cyclically in accordance with a crest function of wavelength equal to one sixth of the synthesised wavelength to produce six crests in synchronism with said portions of the synthesised signal, the peak value of the bus potential being associated with the peaks of said crest function and a lower intermediate level of the bus potential being associated with troughs of said crest function.

7. A supply synthesis arrangement as claimed in claim 6 in which the lower intermediate limit of bus potential is substantially 87% of the upper potential limit.

8. A supply synthesis arrangement as claimed in claim 6 or claim 7 in which the crest generating means comprises a clock, a counter of clock pulses, memory means responsive to different counter levels to access different addresses within the memory, data at each address representing an incremental step of a part of the crest function subsidiary counter means operable to count the incremental steps of the crest function waveform produced by the memory, D/A conversion means operable to convert the instantaneous count level of the secondary counter to an analogue voltage representative of the instantaneous magnitude of the crest function and potential dividing means operable to vary the d.c. supply voltage from its upper level in accordance with the analogue crest function representation.

9. A supply synthesis arrangement as claimed in claim 8 in which the relationship between counter levels and memory addresses containing incremental step data varies sinusoidally to produce said crest function.

10. A supply synthesis arrangement as claimed

in claim 8 or claim 9 in which the subsidiary counter comprises an up-down counter to which the stored increments are applied and count sense gating means responsive to memory address counter levels indicative of ascending or descending parts of the crest function waveform to direct the incremental steps produced by the memory to the respective count-up or count-down input of the subsidiary counter.

11. A supply synthesis arrangement as claimed in any one of claims 8 to 10 when dependent from claim 4 in which the clock and counter are common to the control means and the crest generating means.

12. A supply synthesis arrangement as claimed in claim 11 in which the memory of the control means and memory of the means are both formed by a ROM.

13. A supply synthesis arrangement as claimed in claim 12 in which the ROM is a 4-bit ROM, one bit representing each of the three load supply voltages and the crest waveform.

14. A three phase supply synthesis arrangement substantially as herein described with reference to and as shown by Figure 5 of the accompanying drawings.

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